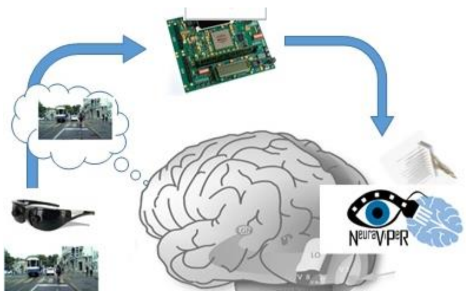
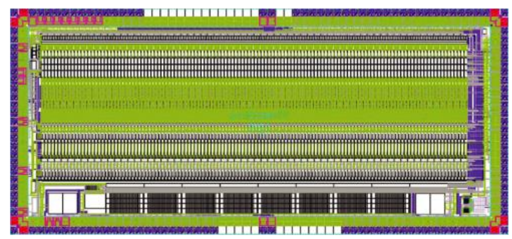
INC-IEM Neuroengineering Seminar

A 128-Channel Real-time Visual Deep Network Stimulation System for a Visual Cortical Neuroprosthesis





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http://sensors.ini.uzh.ch/

Tuesday, January 9, 2024
5:00-6:00pm
Fung Auditorium, Powell-Focht Bioengineering Hall
University of California San Diego

Zoom: https://ucsd.zoom.us/j/2888083696

Abstract: With new developments in electrode and nanoscale silicon technology, it is becoming viable to build a large-scale multielectrode cortical neural prosthesis with thousands of stimulation and recording sites. In the context of a visual neuroprosthesis, a rudimentary form of vision can be presented to the visually impaired by stimulating the electrodes to induce phosphene patterns. In this talk, I present two aspects of joint work from the multi-consortium EU-funded NeuraViPER project (www.neuraviper.eu) in developing a cortical multi-electrode neural prosthesis with the aim of restoring visual perception in visually impaired subjects. The first tackles the challenge of rapid decoding of neural recordings for a closed-loop stimulation system. We report results from applying deep networks on a partner's dataset of 1024 electrode recordings collected from a primate performing a visual discrimination task. The peak decoding accuracy from the V1 data can be obtained by a moving time window of 150 ms, whereas the peak accuracy from the V4 data is achieved at a larger latency and by using a larger moving time window of 300 ms. The second part describes the development of a Visual Prosthesis Convolutional Neural Network (VPCNN) field-programmable gate array (FPGA) accelerator that generates a sparse but informative stimulation pattern output. The VPCNN can be interfaced to a partner's 128 channel stimulation application-specific integrated circuit (ASIC) where the patterns are converted into current pulses to drive a multi-electrode array. Experimental results from the VPCNN show that a 94.5K parameter 14-layer CNN receiving camera frames has an inference rate of 83 frames/sec and uses only an incremental power of 0.1 W, which is at least 10× lower than that measured from an embedded graphical processing unit (GPU) device, the Jetson Nano. Future plans are to implement the equivalent CNN ASIC for even lower power consumption.

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